

The **DEFINITIVE GUIDE** to
CONNECTED INNOVATION INTELLIGENCE for
SEMICONDUCTORS

patsnap

Executive Summary

The semiconductor industry is ripe with growth, challenges, and unprecedented opportunities. Currently worth \$555.9 billion dollars, the industry is expected to reach a \$601 billion dollar valuation by the end of 2022. Although growth is on the horizon, so are industry-wide challenges. Market volatility, intellectual property security issues, and rapid technological advancements make it difficult for semiconductor organizations to stay ahead of emerging trends and out-innovate competitors.

This definitive guide provides an in-depth analysis of the current challenges facing semiconductor professionals and organizations, and how they can leverage Connected Innovation Intelligence (CII) to navigate and overcome these issues.

Powered by Artificial Intelligence (AI), CII provides users with access to millions of regularly updated data points sourced using best-in-class algorithms and expert manual curation. From patent insights to financial news, market and research reports, academic studies, and beyond, CII enables users to explore industry trends and portfolio shifts, improve innovation pipeline, and uncover real-time insights on new research and technology areas. Equipped with accurate, timely insights, the probability of success increases, and resource waste decreases.

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Introduction

Semiconductors power the modern world. These compact and powerful chips are responsible for the Information Age and can be found virtually everywhere – including in smartphones, computers, appliances, automobiles, and medical devices. As such, it comes as no surprise the industry is an economic powerhouse, worth a whopping \$555.9 billion dollars as of 2021, up 26% from 2020. The market is poised for significant growth this year as well, with the [Semiconductor Industry Association](#) (SIA) predicting the industry valuation will reach \$601 billion dollars by the year's end.

This unprecedented growth is due in large part to COVID-19, which ushered in remote work alongside the temporary closure of fabrications plants (also known as 'fabs'), where semiconductors are made. As consumers rushed to upgrade their electronic devices and home entertainment systems, and chip production shut down, demand exceeded supply.

Additionally, geopolitical tensions, especially related to the United States and China, as well as shifting business models for semiconductor production, the rise of the Internet of Things (IoT), and advanced, AI-powered technologies have also contributed to supply chain issues. This combination created the perfect storm of "supply versus demand" and led to a global chip shortage impacting businesses and consumers alike.

This shortage is not without cost. For example, the global automotive industry lost around \$210 billion dollars of revenue in 2021 and produced eight million less vehicles than planned. On the consumer side, continued delays and price increases are expected.

Organizations vying for a piece of the multi-hundred-billion-dollar semiconductor pie must learn how to out-innovate their competitors while at the same time working to overcome the above challenges. Fortunately, technological advancements in AI and machine learning are making it faster and more efficient for semiconductor professionals to analyze competitor patent activity, uncover whitespace, evaluate key industry players, and make more informed business decisions.

As technology continues to evolve at a rapid pace, thanks to artificial intelligence (AI) and the IoT, semiconductors will continue to grow exponentially. In addition to powering the Information Age, semiconductors also fuel the economy.

Digital-based goods, worth \$0.4 trillion in 2020 and account for 22.5% of global GDP, are expected to increase to one trillion dollars by 2035. This growth wouldn't be possible without semiconductors.

The bottom line: without semiconductors, we wouldn't have the modern (and lifesaving) conveniences we've come to rely on.

In this Definitive Guide to Connected Innovation Intelligence (CII) for the Semiconductor Industry, we explore:

- 1. What CII is and how it helps semiconductor professionals**
- 2. The 3 biggest challenges semiconductor professionals face**
- 3. How to leverage CII to accelerate semiconductor innovation**

Part 1: What is CII?

CII is the process of using AI-powered technology to comb through millions of global data points, segment them by industry and relevance, and connect them together in a way that makes sense. This process enables users to quickly sift through vast amounts of data, correlate relevant information, and gain a 360-degree view of a topic, such as a company, an industry, a technology area, or an entire market.

Equipped with accurate data, intellectual property (IP), R&D, and legal professionals can:

- Simplify complex search results and extract meaningful insights
- Conduct high-level market analysis
- Identify early-stage innovation opportunities
- Explore industry trends and competitor portfolio shifts
- Uncover real-time insights on patent activity, new research, and technology areas
- Improve innovation pipeline

PatSnap is a rapidly growing platform for innovation intelligence and an example of true CII. Through PatSnap's AI technology — including machine learning, computer vision, and Optical Character Recognition (OCR) — users have access to an unrivaled breadth of data that is connected in a meaningful way. These connected insights provide innovators with a clear understanding of the market implications, possibilities, and opportunities.

Connected Innovation Intelligence for Semiconductor Professionals & Organizations

CII for IP Professionals

The intellectual property (IP) landscape for the semiconductor industry is multifaceted and complex. A single chip can be patented in a variety of ways due to its unique fabrication process and purpose. As a result, uncovering IP trends can be difficult (at best) without expert-level knowledge and years of experience. In the past, filing, prosecuting, and monitoring patent applications was a manual process for both the applicant and the attorney. In addition to being time-consuming, this approach was also costly and demanding.

However, as technology rapidly advances and AI-powered technology dominates the market, searching, analyzing, and monitoring industry developments (as well as global IP processes) is easier than ever. With CII, IP professionals gain access to simplified keyword searches, thereby empowering them to efficiently identify relevant IP documentation. Additionally, sophisticated classification searching and filtering aids in removing irrelevant records from search results, helping professionals uncover IP relevant to their specific projects.

Thus, companies can make more informed decisions concerning investments, minimize the threat of litigation and look for opportunities to license, sell, or buy IP assets. These actions can be achieved by looking at insights, metric representations, and collaborating with colleagues and global IP offices with just one click of a button. Plus, companies can move more IP work in-house, thereby reducing cost, saving time on searches, and collaborating via workspaces which enables organizations to avoid the duplication of work.



Connected Innovation Intelligence for Semiconductor Professionals & Organizations (Cont'd)

CII for R&D Professionals

Due to rapid technological advancements, as well as short product life cycles (think the Apple iPhone), R&D professionals need to have a keen understanding of industry trends, particularly concerning where technology is headed. Otherwise, it will be difficult at best, and impossible at worst, to launch new chip innovations in a timely manner.

According to a [McKinsey](#) study of more than 2,000 integrated-circuit projects, "...companies often drastically underestimate staffing requirements and have to play catch-up later in the life of a project." Additionally, this report mentioned companies often miss deadlines and overspend budgets. As a result, competing organizations that work faster and more efficiently can begin taking on more market share.

With CII, R&D professionals can leverage AI-powered semantic search and access relevant patents and scientific literature to streamline the research process.

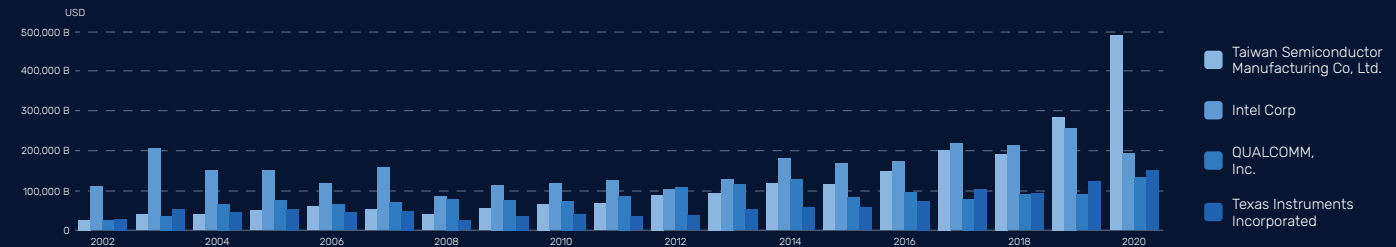
Additionally, researchers can comb through millions of scientific literature trends, grants, tech blogs, market and commercial insights, and patent activity to identify whitespace, perform in-depth analysis and stay ahead of emerging trends.



Case Study: TSMC



Market Cap



The Taiwan Semiconductor Manufacturing Company (TSMC) is an excellent example of what happens when R&D falls behind, and specialized organizations take the lead.

Founded by Dr. Morris Chang (often referred to as “the father of semiconductors”) in 1987, TSMC began as a collaboration between the Taiwanese government, tech giant Philips, and a handful of investors. The business plan — to focus only on manufacturing chips for other industries (known as a ‘foundry’), was disruptive and met with industry-wide skepticism. At the time, Intel and Texas Instruments dominated the market. Both organizations designed and manufactured their own chips.

However, Dr. Chang saw something other companies didn’t — he recognized the rapid pace of technological change, and predicted companies wouldn’t be able

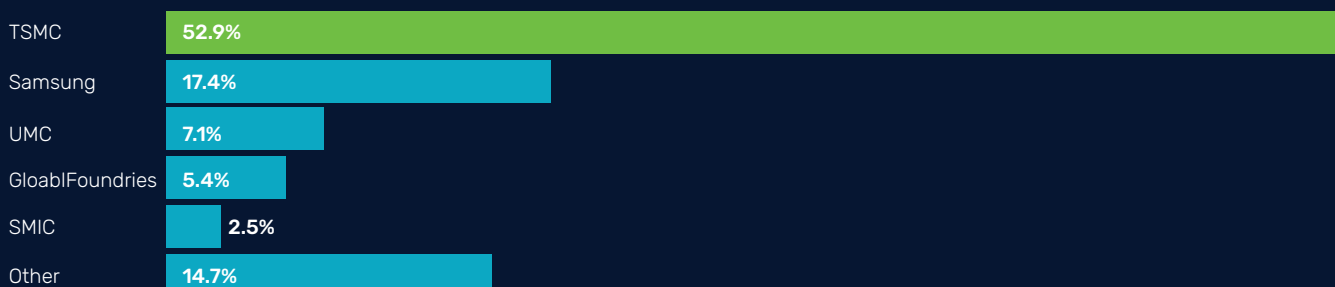
to continue launching new innovations while also manufacturing their own chips.

Today, TSMC leads the foundry industry and is one of two companies capable of making the most advanced, 5-nanometer chips found in the latest smartphones. Additionally, Intel outsources some of its chip production to TSMC, and Apple relies on it for every iPhone.

Now a tech giant, TSMC’s story comes with a warning for organizations currently dominating the market: disruption is just around the corner. To remain competitive, R&D professionals must leverage data to keep a pulse on industry trends and market shifts, otherwise they’ll be ill-equipped to make predictions about where the market is headed, resulting in resource waste and loss of market share.

TSMC has more than half the contract chip manufacturing market

Contract chip foundry market share % by revenue, Q2 2021



Source: Investment Monitor

Taiwan Semiconductor Manufacturing Company (TSMC) holds the majority of market share in the contract foundry area. TSMC is Asia’s highest valued company at \$600B USD.

CII for Fabrication Sites

A fabrications plant, or 'fab' for short, is a manufacturing plant where raw silicon wafers are turned into integrated circuits (IC). This process takes place in a highly controlled environment equipped with a state-of-the-art air ventilation system to prevent dust particles from contaminating the chips.

In addition to being high maintenance, fabs are also expensive to build and sustain. Depending on the fab type, constructing a new site can cost anywhere between \$1.5 billion dollars to more than \$10 billion dollars and take several years to complete. Furthermore, increased equipment costs coupled with inflation are adding to the global chip shortage. As technology continues to advance, and industries require smaller, faster chips that use less power, more fab sites will need to be built or updated to meet this demand.

For example, 200mm wafer capacity manufacturing remains in [high demand](#) on the consumer side but has very few fab sites. While key events in the global economy result in semiconductor supply chain shortages, the 200mm wafer remains the highest in demand. Despite this, there are global plans to build 24 new 300mm wafer fab plants in 2022, but only 10 new 200mm fab plants. If these plans are approved, supply shortages will continue. What's more, these fab plants are geographically clustered in dense areas. In fact, the US, Taiwan, South Korea, Japan, and China, make up nearly 60% of the chip making concentration.



Top 4 Foundries Application Filing Trends, Last 10 Years

However, large multinational enterprises are now pushing for the ["localization"](#) of their fabrication plants, as the uncertainty of supply chains can have an adverse impact on revenue. The just-in-time production of semiconductor chips, where fabrication plants account for bulk requests related to demand, will soon be a trend of the past. Large organizations such as Apple and Tesla are moving away from this model in favor of pre-purchasing to avoid loss in revenue.

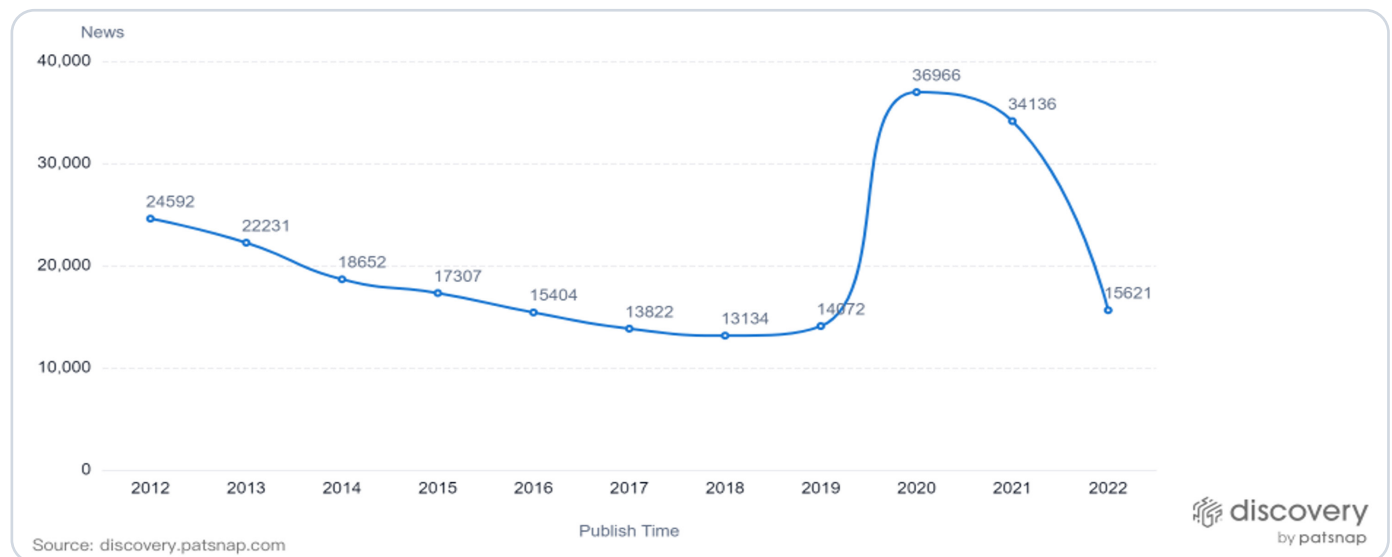
With CII, an organization looking to build a new fab site or expand upon an existing one can conduct more diligent, thorough research prior to the decision-making process. For example, when determining how to design for the future – including what companies are leading the charge (such as those illustrated in the chart above which details the top four foundries based on application filing trends over the past 10 years) and what materials to use for new innovations, global data can be analyzed including patent information, technology news, investment data, merger and acquisition activity, and more. Equipped with these insights, organizations can make better predictions about the future, and how to remain competitive.

Part 2: Current Challenges Facing the Semiconductor Industry

Challenge 1: Market Uncertainty & Volatility

From geopolitical tensions between the US and China, to uncertainties about the future of post-pandemic life, market uncertainty and volatility represents a major challenge for semiconductor professionals and organizations alike.

When the COVID-19 pandemic first emerged in 2020, the industry noted higher-than-normal demands for personal devices like smartphones and laptops. Worldwide [PC shipments](#) grew by 4.8% in 2020 (noting a 10.7% increase in the fourth quarter) resulting in the highest global PC growth in more than a decade.



As the demand for consumer electronics skyrocketed due to the COVID-19 pandemic, so did news coverage highlighting the newfound demand for these products (laptops, tablets, cellphones). The chart above showcases mentions in the news, which increased nearly 200% from 2019 to 2020.

Even as life returns to “normal,” remote work is here to stay. According to a recent [PEW Research Center survey](#), 60% of US workers indicated they want to continue working from home, regardless of whether their offices reopen. Many employees who aren’t given the option to continue telecommuting are quitting, ushering in a new age of work.

While this is good news for the industry, because it guarantees strong sales and growth for consumer electronics, it’s also challenging. To capture market share, semiconductor organizations need to have a strong grasp on how the marketing is trending

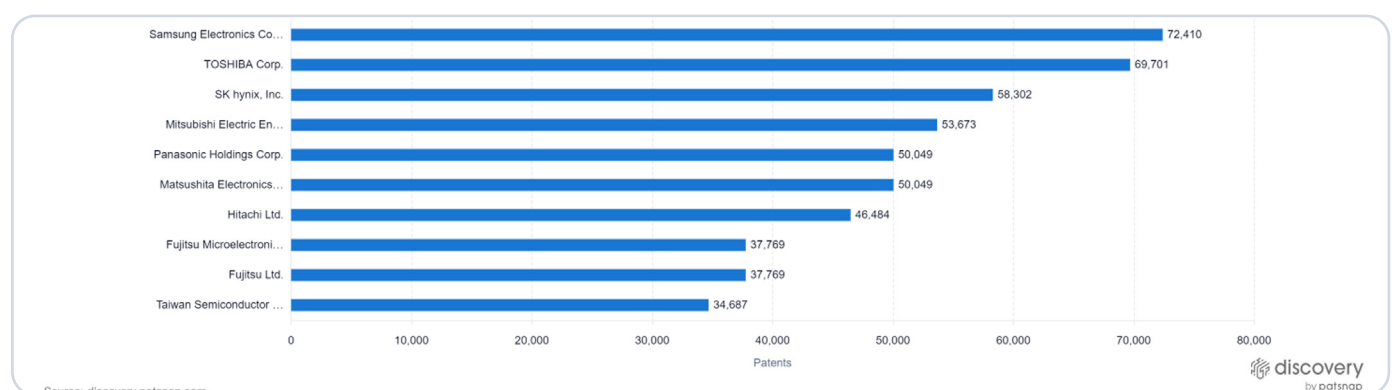
— including what technological advancements are underway, to make the right investments in research and development. In the absence of predictive analysis, organizations will fall behind.

Additionally, if tensions between the US and China continue, semiconductor organizations may experience disruption in the supply chain. To mitigate that risk, Taiwan-based TSMC (which owns 53% of the global market share) is building a factory in Phoenix, Arizona which is expected to begin production in 2024.

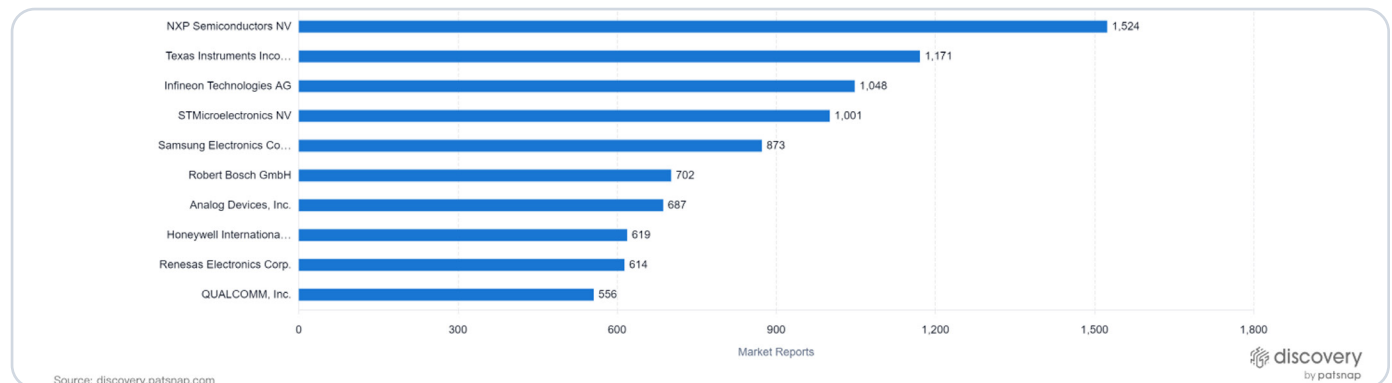
As opposed to taking a “wait and see approach,” organizations can be proactive and leverage CII to gain a better understanding of how the market is trending and who the key players are.

Below, we’ll walk you through an example of CII in action. We ran several searches, including a technology and market search to uncover key players, patent activity, and the fastest growing sectors.

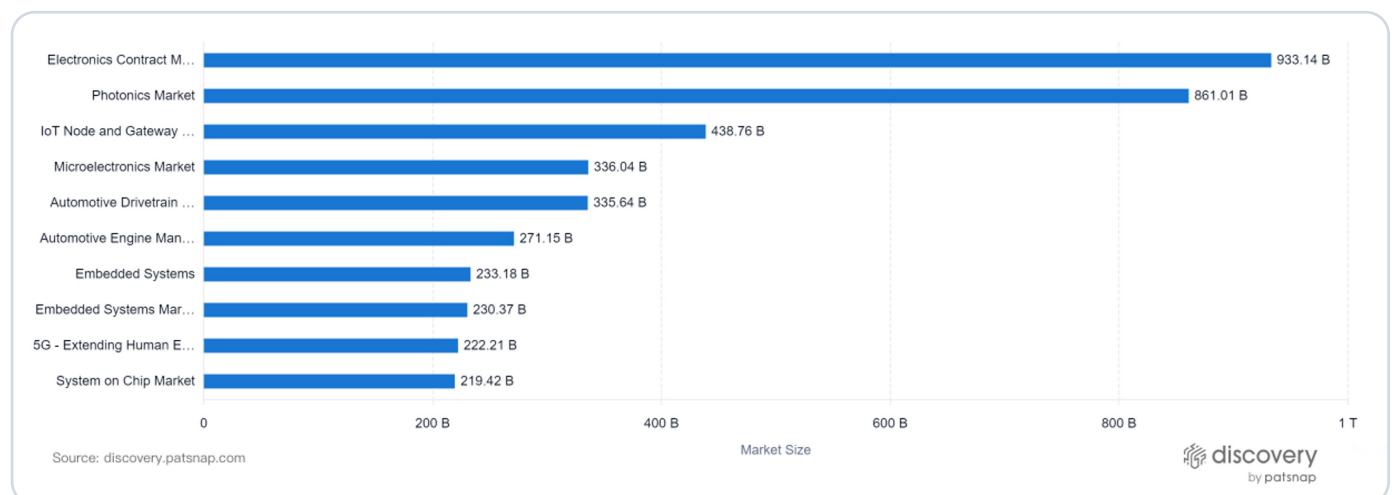
Starting with the technology search, we can quickly identify the top patent holders in this space. In this case, Samsung, Toshiba, and SK Hynix lead.



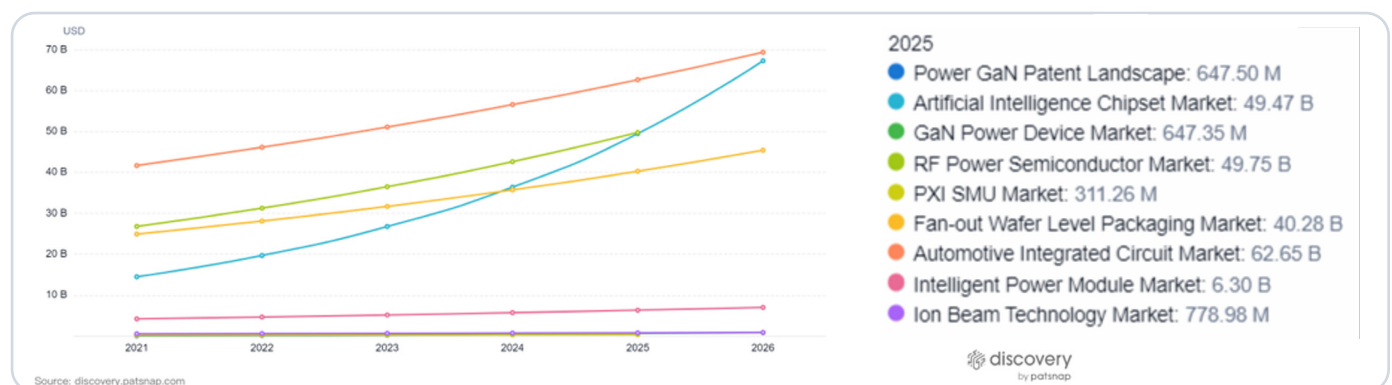
In the market analysis report on semiconductors below, the companies mentioned most often in reports are outlined. These insights highlight key players in the space to monitor.



Drilling further, we uncover the largest global market sectors currently dominating the industry. Unsurprisingly, electronics contract manufacturing leads with a valuation of \$933.14 billion dollars, followed closely by the photonics market with a \$861.01 billion dollar valuation.



In terms of market projections, we can run a quick analysis to highlight the fastest growing sectors, uncover their CARG as well as projected valuations for a given time period. In this analysis, we see the markets expected to have the highest valuation by 2025 are Automotive Integrated Circuits, Artificial Intelligence Chipsets and RF Power Semiconductors.

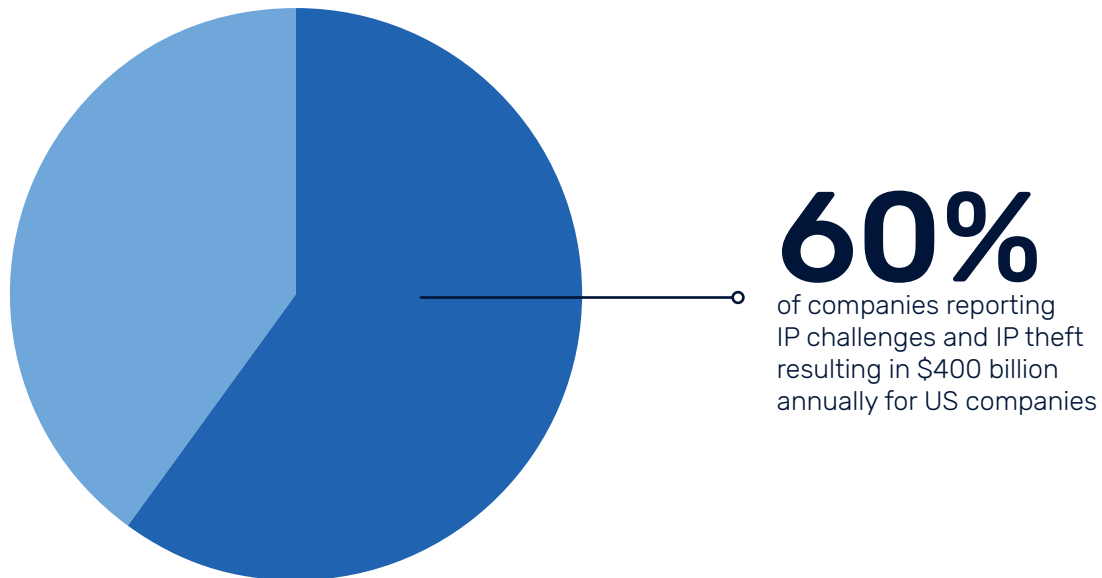


These insights can be drilled down further and analyzed to extract relevant information, uncover key market happenings, and inform strategic business decisions.

Challenge 2: IP Security

According to the SIA, research and development investment in the US semiconductor industry is one of the costliest sectors. It's also one of the most infringed. SEMI, an organization dedicated to serving the design and manufacturing chain for the electronics industry,

conducted a survey and found more than [60% of semiconductor companies](#) report IP challenges have had a negative impact on their bottom line. Organizations mentioned patent infringement and counterfeiting as the primary concerns.



The risk of IP theft is exacerbated by the fact that many chip companies serve other industries, and as a result, improper handling of trade secrets, patent data, and IP theft often occurs. Additionally, global technology transfers can be risky for certain organizations and cost billions of dollars. According to the US IP Commission, theft from Chinese companies or state-owned enterprises accounts for economic losses in the US of more than \$400 billion dollars annually.

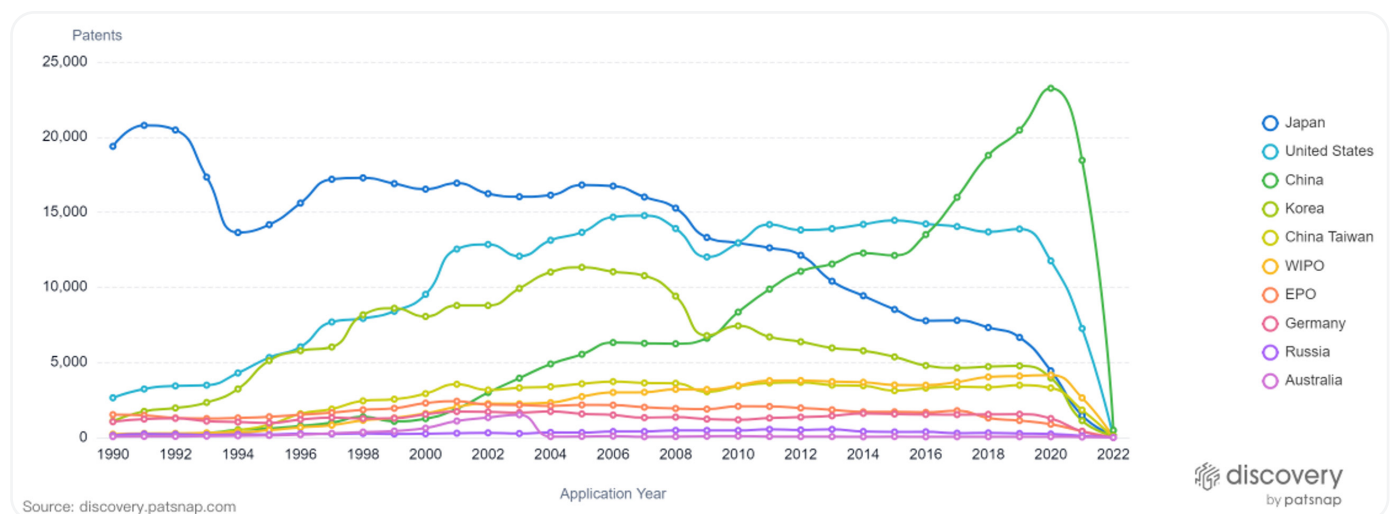
As such, IP security is a real challenge for organizations. To reduce the likelihood of infringement, proactive risk management – including monitoring patent activity, is a crucial part of the overall IP defense strategy.

Challenge 3: Rapid Technological Advancement

The chip industry is one of the fastest-paced, most R&D-intensive sectors in the world. [Moore's Law](#), coined by Intel's co-founder Gordon Moore, states the number of transistors in a dense circuit will double (in speed and processing capabilities) approximately every two years. Meanwhile, costs will be cut in half. Thus far, the accuracy of Moore's Law has been spot-on as the number of transistors per wafer has increased by about 10 million since its introduction in 1975.

However, experts (including Gordon Moore himself) expect this law to become invalid by 2025.

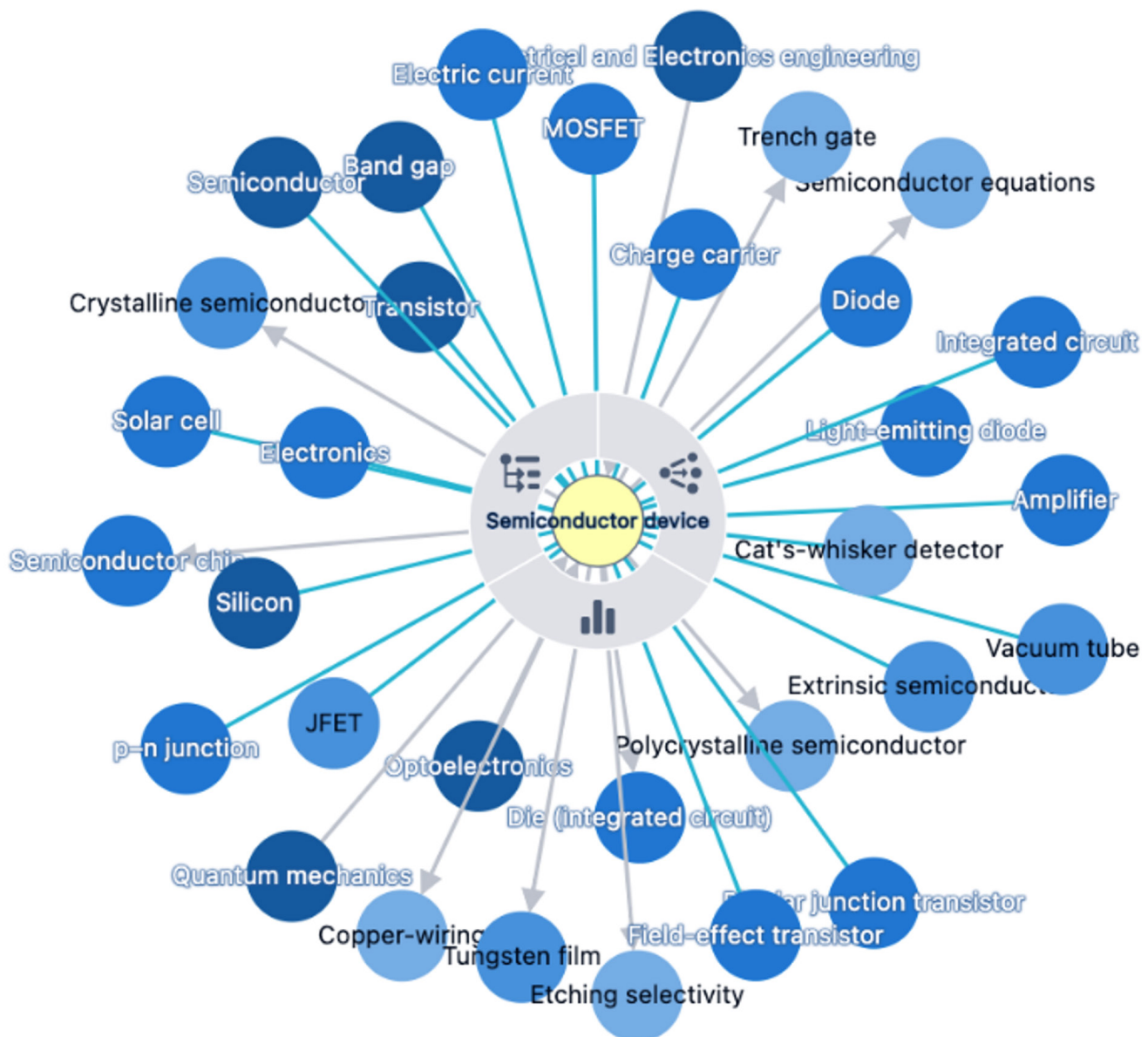
The reality is, as chips become smaller and technology more advanced, it's hard for organizations to keep up. For example, in the 1990s, the US owned 37% of the global semiconductor manufacturing market. Today it owns just 12%.



In the early 1990's Japan, followed by the US, were the top patent holders in the semiconductor industry. As of the late 2000's, there has been a pivot with huge increases in patent filings in China, resulting in them surpassing both Japan and US.

What's more, in July 2020 Intel announced it was about a year behind in developing the next generation of chip technology. The bottom line is research and development in the semiconductor sector is difficult, time-consuming, and full of challenges.

Academic research maturity: low  high



Academic research trends for semiconductor devices, PatSnap Discovery

Accelerating innovation means having access to data that enables professionals to predict market shifts, uncover emerging trends, identify whitespace, and seamlessly collaborate to avoid the duplication of efforts.

“

60% of semiconductor companies report IP challenges have a negative impact on bottom line. To maximize ROI on innovation while proactively managing risk, innovation intelligence strategies – such as monitoring patent filing and other innovation activity in geographies that are critical to chip manufacturing – must be deployed throughout the enterprise.

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Part 3: _____ How to Accelerate R&D & Reduce IP Risk with CII

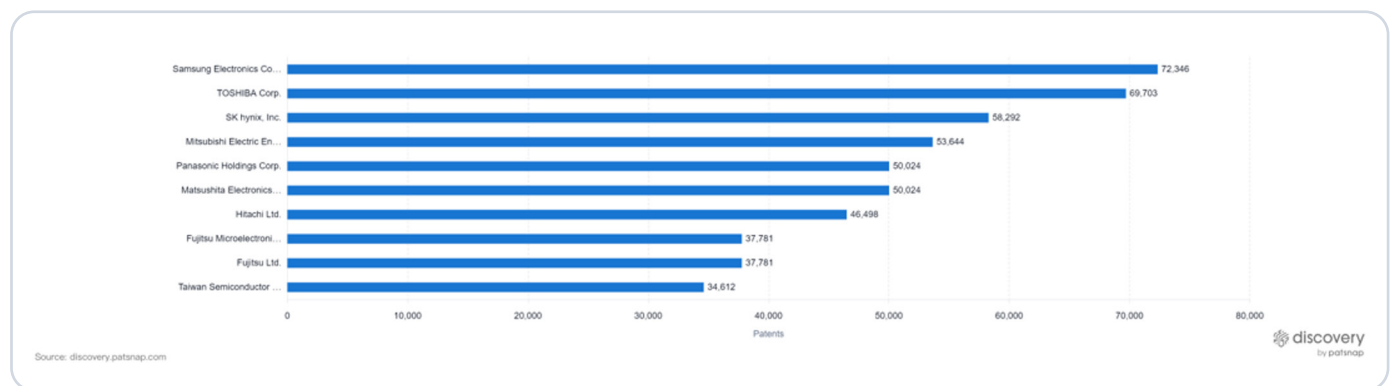
In a time of exponential growth, and global uncertainty, streamlining the research and development process and accelerating innovation is key to remaining competitive. In this section, we'll show you how to leverage CII to overcome the challenges listed above, expedite R&D, protect IP, and expedite innovation.

Using CII to Uncover Semiconductor Market Trends

Earlier, we discussed how market volatility coupled with fast-paced technological advancements make it difficult for semiconductor organizations to build and sustain viable businesses. Now, we'll demonstrate how to use CII to keep a pulse on market shifts, competitor activity, technology trends, partnership opportunities, and emerging players.

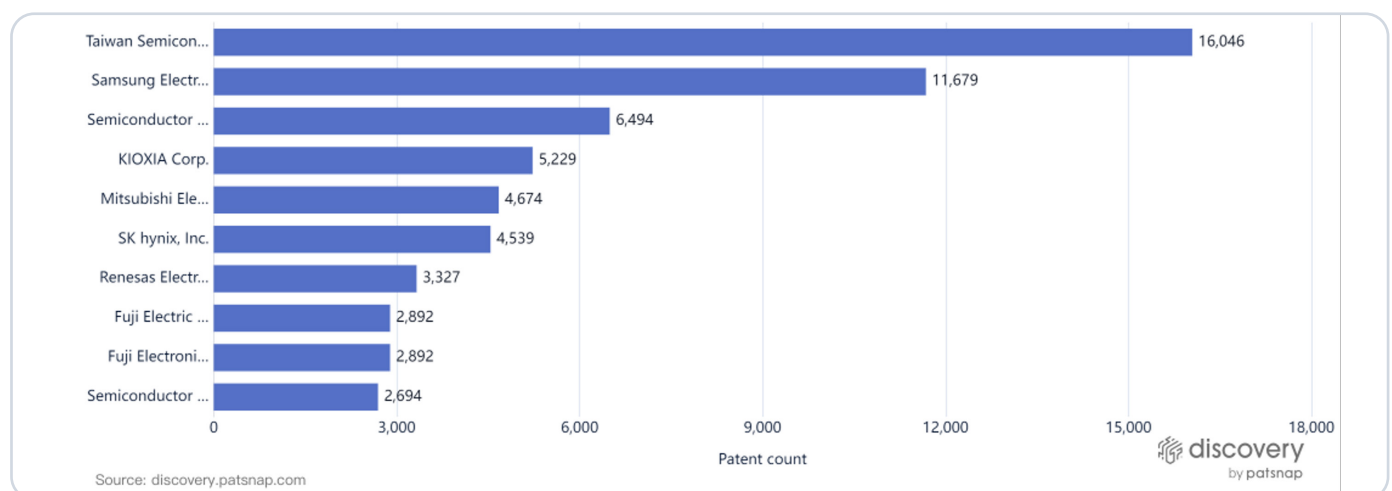
With CII, you uncover and connect various data points to answer business-altering questions such as, "What trends are likely to impact supply and demand in the future?" and "What are our competitors doing (and why)?"

Monitoring Competitor Activity



With CII you can monitor competitor activity with ease. For example, in the chart above we ran a patent portfolio search to understand which companies dominate the patent sector in this space. Based on our findings, we see Samsung Electronics, Toshiba Corp, and SK hynix Inc. Are the top three companies with the largest semiconductor patent portfolios.

Based on these findings, you can set an alert to track the patent activity of these three companies or all of the major players. This way, you can easily keep track of patent portfolio changes.

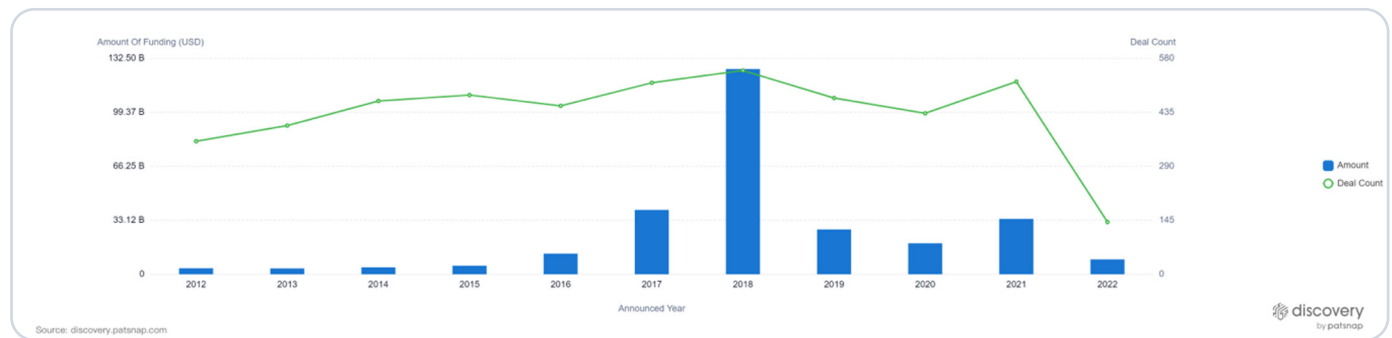


You can also analyze the patent applications over a set amount of time. In the analysis above, organizations applied for 255,166 semiconductor related patents over a five-year period. This search illustrates the fastest-growing patent holders, including Taiwan Semiconductor Manufacturing, Samsung Electronics,

and Semiconductor Energy Laboratory, which account for 13.41% of the patent filing during this period.

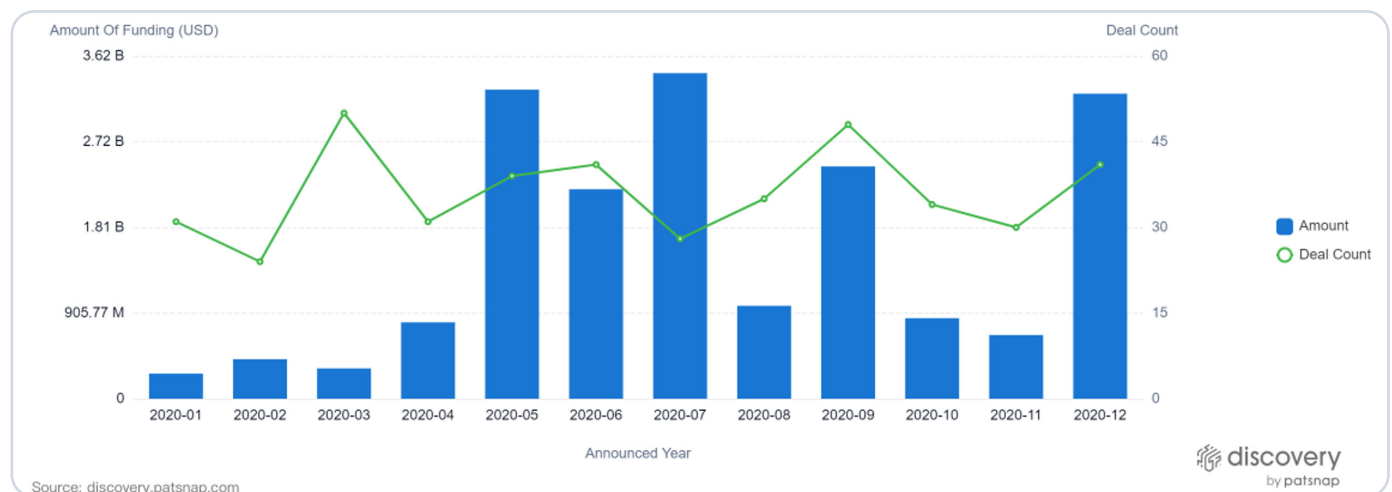
Data such as this will help you identify key players, as well as emerging organizations.

Uncovering VC Investments, M&A Activity, and Patent Data



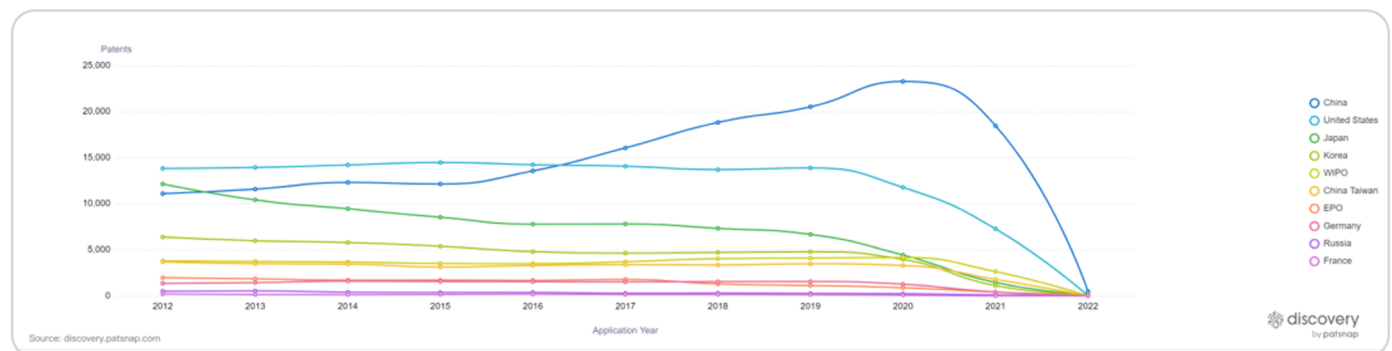
If you're interested in understanding VC investments, M&A activity, or financial data in general, Discovery can help with that, too. In this example, we are specifically interested in investment history over the past decade so we can understand how the financial market is trending.

Notably, this graph shows a record-breaking investment of \$100 billion in 2018 from seven banks to US chipmaker Broadcom. This investment aided in their proposed \$117 billion acquisition of Qualcomm; however, the deal never came to fruition as former President Donald Trump blocked the deal due to national security concerns.



Discovery can also help you keep a pulse on market volatility. In the case of semiconductors, the onset of the COVID-19 pandemic led to a dramatic increase in investments (as shown above).

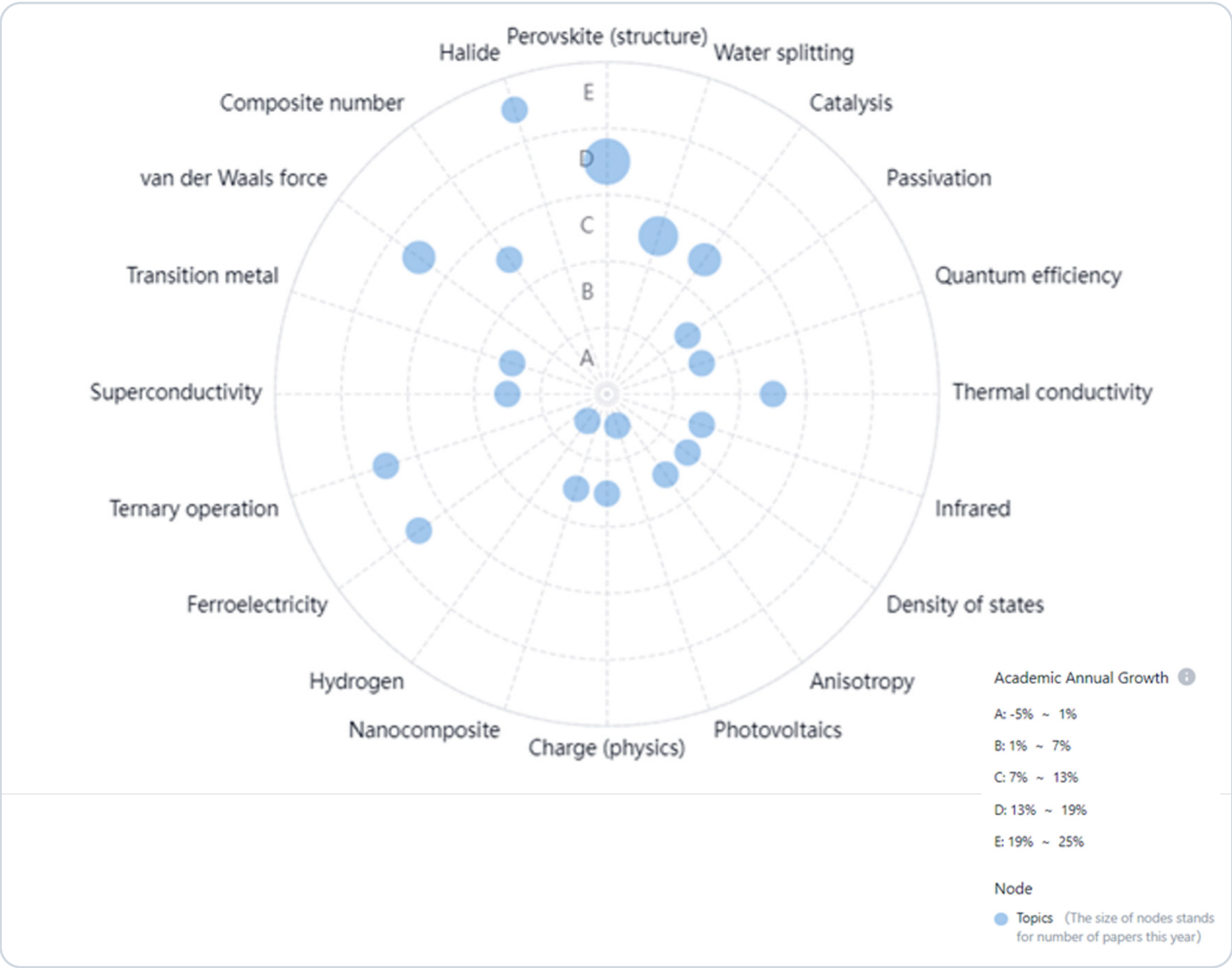
This trend went hand-in-hand with non-essential employees working from home and updating their electronic devices such as laptops and phones as a result.



Additionally, we can run a jurisdiction analysis to understand which countries are leading the industry now, versus which countries will lead in the future.

In the semiconductor industry, China leads with patent applications, which corresponds with China's plans to dominate the global chip market by 2025.

Discovering Emerging Trends



With CII, you can also uncover new technologies and analyze how those technologies may disrupt the future of the industry. For example, the graph above compares emerging technologies in the semiconductor space to academic literature published over the past three years.

As illustrated, Halide (Metal-halide semiconductors or MHSs for short) has a three-year academic growth rate of 22.8% with 308 papers published. The research areas with the most academic papers (as indicated by node size) are the most popular topics in this technology space.

In the semiconductor space, Perovskite structures is the topic written about the most in academic studies, with 903 papers in total.

Other high-growth categories include van der Waals force, Ternary operation, ferroelectricity, and water splitting.

These insights allow you to be at the forefront of technological advancements, identify potential partners, and regularly assess or adapt your innovation strategy.

Protecting IP and Increasing Search Efficiency with CII:

Lack of IP protection costs semiconductor companies billions of dollars annually. As such, monitoring infringements and maintaining a rigorous protection strategy are of the utmost importance.

With CII, IP professionals can move beyond just patent search and refinement, and leverage tools that streamline patent protection. In this section, we'll explore a handful of relevant tools and showcase how they work.

Advanced Searching with CII:

In contrast to traditional searching, which makes it difficult to find keywords or get an accurate depiction of the market, CII empowers users to simplify complex search results and extract meaningful insights. Using PatSnap's "Advanced" search tool, users can quickly define what they're looking for.

Advanced

☒ Patent type

☒ Applications
 ☒ Patents
 ☒ Utility models
 ☒ Designs

☐ All databases (1/158)

☐ IP 5

☒ United Stat... (US)
 ☐ China (CN)
 ☐ EPO (EP)
 ☐ Japan (JP)
 ☐ Korea (KR)

Field search

Search Helper

Save template

⚙

Main Fields

Semiconductor devices

Keyword Helper

AND

All Assignees

TREE@"SAMSUNG ELECTRONICS CO LTD"

Corporate Tree

AND

IPC

G03F

IPC Helper

+ Add Field

((Semiconductor devices) OR TACD_ALL:(Semiconductor devices)) AND ALL_AN:(TREE@"SAMSUNG ELECTRONICS CO LTD") AND IPC:(G03F)

Edit search

Combine searches

Save Query

Found 1,630 patents

Includes Machine Translations ☒

Clear

Search

Advanced search empowers professionals to create a piece-by-piece query, and select the main fields and keywords needed to conduct a proper analysis. This process provides users with rigorous control of the search, thereby producing accurate, relevant results.

Keyword Helper

×

semiconductor

Analyze

semiconductor

iii-v

compound semiconductor

iii-group

nitride-based

p-type

gan

n-type

epitaxial

gaas

compound semiconductor element

compound semiconductor substrate

iii-family

group-iii

semiconductor material

group compound semiconductor

compound-semiconductor

different semiconductor

first semiconductor

silicon-germanium

sapphire substrate

CN

EN

Select the relevant option from the left and click submit

Additionally, the "Keyword Helper" is designed to provide users with relevant terms for searching. In the example above, by using "semiconductor" as a search term, various other related terms are also offered to help expand search criteria and accuracy, thereby reducing the likelihood of missing important information.

CII Search Refining:

In the semiconductor space, it's easy to become overwhelmed by the vast amount of data available. For example, when conducting freedom to operate (FTO) searches, researchers need to sift through all relevant prior art and patent data.

Unfortunately, this is easier said than done. Separating relevant versus irrelevant information is time-consuming and tedious. But it doesn't have to be. With CII, it's easy to refine thousands (or more) search results down to the most applicable patents. One of the most common filters is the simple legal status of a patent – if a patent is inactive, it cannot be used as a prevention tool, giving others clearance with the technologies mentioned.

Another useful refinement is by IPC or CPC code – this allows you to focus your search on a particular application. By using this refinement, you can uncover commercialized innovations and make practical predictions about future progress in an area.

A final common refinement is by assignee. This will allow you to see active players and organizations within your field. Additionally, it enables you to identify potential licensing partners, as well as primary (or up-and-coming) competitors.

The screenshot displays the CII search interface with a list of patents. The interface includes a sidebar with filters for Assignee, Authority, and Application Year. The main table shows patent details including Publication Number, Title, Legal Status, Std. Current Assignee, and Application Domain.

Filters:

- Assignee:** SHANGHAI CAMBRICON INFORMATION TECH CO LTD (544), INTEL CORP (460), GOOGLE LLC (454), CAMBRICON TECH CO LTD (353), SAMSUNG ELECTRONICS CO LTD (339), IBM CORP (305), NVIDIA CORP (253), MICRON TECH INC (210), HUAWEI TECH CO LTD (163), SEMICON ENERGY LAB CO LTD (142).
- Authority:** China (3967), United States (3568), WIPO (1127).
- Application Year:** 2021, 2020, 2019.

Patent List:

Publication Number	Title	Legal Status	Std. Current Assignee	Application Domain
1 • US20210312271A1	Edge ai accelerator service	Examining	VMWARE INC	Concurrent instruction execution, Physical realisation, Data switching networks
2 • US9792547B2	Neural network circuit and learning method for neural network circuit	Granted	PANASONIC INTELLECTUAL	Neural architectures, Physical realisation, Neural learning methods
3 • US20150269483A1	Neural network circuit and learning method for neural network circuit	Granted	PANASONIC INTELLECTUAL	Digital computer details, Neural architectures, Physical realisation, Neural learning methods, Electric digital data processing
4 • US20190114538A1	Host-directed multi-layer neural network processing via per-layer work requests	Examining	XILINX INC	Operational speed enhancement, Neural architectures, Physical realisation, Neural learning methods, Logic circuits using elementary log, Complex mathematical operations
5 • US9928460B1	Neural network accelerator tile architecture with three-dimensional stacking	Granted	GOOGLE LLC	Neural architectures, Physical realisation, Transmissi
6 • US2018036553A1	Neural network accelerator tile architecture with three-dimensional stacking	Withdrawn	GOOGLE LLC	Neural architec, Help, Physical realisation

39 filtered records. Undo

YOUR SELECTED FILTERS:

- AND Application Year: 2021, 2020, 2019
- AND Authority: United States
- AND IPC Sub Group: G06K9/62
- AND MIPC Group: G06N3

Patent List (Filtered):

Publication Number	Title	Legal Status	Std. Current Assignee	Application Domain
1 • US20210110243A1	Deep learning accelerator system interface	Examining	HEWLETT-PACKARD ENTER	Program synchronisation, Character and pattern re, Concurrent instruction ex, Neural architectures, Inference methods, Ph
2 • US20200134416A1	System-on-a-chip incorporating artificial neural network and general-purpose processor circuitry	Examining	ELECTRONICS WARFARE AS	Digital data processing d, Digital computer details, Character and pattern re, Speech recognition, Neural architectures, Physical realisation, Energy efficient computr, Neural learning methods
3 • US20220019897A1	Deep neural network training accelerator and operation method thereof	Published	KOREA UNIV RES & BUSINES	Resource allocation, Character and pattern re

Take the image on the previous page as an example. Let's say you're interested in finding out more about the semiconductor patents associated with AI. Using relevant refinements, you can reduce the initial search result featuring 12,754 patents by adding filters. In this case, perhaps you want to search by jurisdiction, application year, legal status, and specific IPC subgroups. These filters narrow your search to results hyper-relevant to your specific needs and provide you with 39 associated records – a much more manageable number that you can analyze for FTO.

The Importance of Collaboration:

Beyond patent searching and reporting, businesses are beginning to understand how important it is to adopt and encourage a culture of collaboration and transparency, allowing for cross-function partnerships. PatSnap's CII platform enables cross-department collaboration in real time with Workspace and simplifies C-suite communication with customized visualizations and graphs.

Collaboration is key as IP and R&D teams need to communicate throughout the innovation lifecycle, otherwise, inefficiencies such as duplication of work can occur. With CII, users can leverage Workspace, integrate their patent strategy, align on priorities, and increase efficiency.

	Publication Number	Title	Applicati...	Legal Status	Current Assignee	Comments	Cited By Co...	Assign to	Importance
1	US20220067509A1	System and method for learning from partial compressed representation	02 Sep 2020	Examining	ALIBABA GROUP HOI	kwhite@patsnap.com: from partial compressed representation	-	Antasha Solomon	High
2	US11250296B2	Automatic generation of ground truth data for training or retraining machine learning models	24 Jul 2019	Granted	NVIDIA CORPORATIC	kwhite@patsnap.com: ground truth data as a result of the object tracking algorithms outputs	-	Antasha Solomon	High
3	US20220019897A1	Deep neural network training accelerator and operation method thereof	19 Jan 2021	Published	KOREA UNIVERSITY		-		
4	US20210406673A1	Interface translation using one or more neural networks	26 Jun 2020	Examining	NVIDIA CORPORATIC		-	kwhite@patsnap.cor	Medium
5	US20210397957A1	Multi-processor training of neural networks	16 Jun 2021	Examining	APPLE INC.	kwhite@patsnap.com: multi processor training	-	kwhite@patsnap.cor	High
6	US20210397930A1	Accelerating binary neural networks within latch structure of non-volatile memory devices	22 Jun 2020	Examining Pledge	WESTERN DIGITAL TI		-	kwhite@patsnap.cor	Low

Workspace also allows users to manage work, capture important records, and generate different analyses and indexing schemes for relevant applications. These insights and observations can then be shared with colleagues and include assigned trackable tasks to be completed. Furthermore, teams can work collectively on a dataset, thereby reducing siloed or duplicated work. This can be used for a variety of internal projects such as managing R&D pipelines, competitors, or external licensing and M&A targets.

Analyzing Patent Records to Extract Meaningful Insights:

CII also allows users to analyze patent records at a granular level and extract meaningful insights about the IP landscape. A few notable capabilities include:

1. Smart image
2. Similar patents
3. Claim comparisons

With smart image search, patent image labels are pulled effortlessly via AI and optical image recognition to provide searchers with a visual map of the patent and explains what the key terms refer to. This enables all professionals, regardless of prior IP experience, to understand what the patents mean.

Start your search with a keyword, company name, patent number etc.

US20210312271A1 **Examining**

Edge ai accelerator service

Abstract

Claims

Description

Images (6)

PDF

Valuation

Legal

Similar Patents (100)

More Similar Patents

Save

Export

Prior Art	Relevancy	Publication Number/Title	Current Assignee	Abstract Image
Post-priority 85% US11269801B2 Granted System decoder for training accelerators Application Date: 17 Dec 2020 Publication Date: 08 Mar 2022 INTEL CORPORATION				
Pre-priority 84% US1120299B2 Granted Transfer Installation and operation of different processes of an AI engine adapted to different configurations of hardware located on-premises and in hybrid environments Application Date: 14 Jun 2018 Publication Date: 14 Sep 2021 MICROSOFT TECHNOLOGY LICENSING, LLC				

Citation

Family

Similar Patents

Related Literature

In conjunction, the “similar patents” feature allows you to pull up to 100 patents like the one you’re viewing. This provides you with a more informed understanding of the technology landscape, including key players, similar research happening, potential risks etc. This process includes calculating patents by keyword similarity, classification code referencing, and backwards citations.

Additionally, with the claim comparison tool you can seamlessly compare the claims and descriptions for members of the same patent family.

US20220088715A1 **Examining**

Semiconductor devices and methods of forming the same

Abstract

Claims

Description

Images

PDF

Compare with KR102011033700A

Compare with US1084388B2

1. A semiconductor device comprising:
a first trench defining a fin, the first trench having a first depth and a first width; a first source/drain region and a second source/drain region on the fin, the first source/drain region and the second source/drain region being adjacent to each other; a second trench in the fin and between the first source/drain region and the second source/drain region, the second trench having a second depth that is different from the first depth and a second width that is narrower than the first width; and a first device isolating layer and a second device isolating layer in the first trench and the second trench, respectively, wherein the second trench comprises a lower portion comprising opposing sides that are laterally bulging.

2. The semiconductor device of claim 1, wherein the first device isolating layer and the second device isolating layer comprise materials different from each other.

3. The semiconductor device of claim 1, further comprising:
a first metal gate on the fin and on a side of the first source/drain region, the first metal gate and the second metal gate traversing the fin and being adjacent to each other;
a first interlayer insulating layer on the first metal gate; and
a second interlayer insulating layer on the second device isolating layer, wherein a height of a bottom surface of the first interlayer insulating layer and a height of a bottom surface of the second interlayer insulating layer are the same.

4. The semiconductor device of claim 1, wherein the second depth is greater than each of a distance between an upper surface of the fin to a lowermost end of the first source/drain region and a distance between the upper surface of the fin to a lowermost end of the second source/drain region.

5. A semiconductor device comprising:
a first trench defining a fin, the first trench having a first depth and a first width; a first metal gate and a second metal gate on the fin, the first metal gate and the second metal gate traversing the fin and being adjacent to each other; a second trench in the fin and between the first metal gate and the second metal gate, the second trench having a second depth that is different from the first depth and a second width that is narrower than the first width; and a first device isolating layer and a second device isolating layer in the first trench and the second trench, respectively, wherein the second trench comprises a lower portion comprising opposing sides that are laterally bulging.

6. The semiconductor device of claim 5, wherein the first device isolating layer and the second device isolating layer comprise materials different from each other.

7. The semiconductor device of claim 5, further comprising:
a first interlayer insulating layer on the first metal gate; and
a second interlayer insulating layer on the second device isolating layer, wherein a height of a bottom surface of the first interlayer insulating layer and a height of a bottom surface of the second interlayer insulating layer are the same.

8. The semiconductor device of claim 5, further comprising:
a first source/drain region on the fin and on a side of the first metal gate; and
a second source/drain region on the fin and on a side of the second metal gate, the first source/drain region and the second source/drain region being adjacent to each other, wherein the second depth is greater than each of a distance between an upper surface of the fin to a lowermost end of the first source/drain region and a distance between the upper surface of the fin to a lowermost end of the second source/drain region.

9. The semiconductor device of claim 5, wherein the second depth is less than the first depth.

10. A semiconductor device comprising:
a first trench defining a fin, the first trench having a first depth and a first width; a first metal gate and a second metal gate on the fin, the first metal gate and the second metal gate traversing the fin and being adjacent to each other; a first source/drain region on the fin and on a side of the first metal gate; a second source/drain region on the fin and on a side of the second metal gate, the first source/drain region and the second source/drain region being adjacent to each other; a second trench in the fin and between the first source/drain region and the second source/drain region, the second trench having a second depth that is different from the first depth and a second width that is narrower than the first width; a first device isolating layer and a second device isolating layer in the first trench and the second trench, respectively, a first interlayer insulating layer on the first metal gate; and a second interlayer insulating layer on the second device isolating layer, wherein the second trench comprises a lower portion comprising opposing sides that are laterally bulging, wherein the second depth is greater than each of a distance between an upper surface of the fin to a lowermost end of the first source/drain region and a distance between the upper surface of the fin to a lowermost end of the second source/drain region, and wherein a height of a bottom surface of the first interlayer insulating layer and a height of a bottom surface of the second interlayer insulating layer are the same.

1. A semiconductor device comprising: a first trench of a first depth defining a fin, a second trench of a second depth that is greater than the first depth, a first gate and a second gate on the fin, the first gate and the second gate traversing the fin and defining a fin, the first trench having a first depth and a first width, a first source/drain region and a second source/drain region on the fin, the first source/drain region and the second source/drain region being adjacent to each other, a third trench in the fin and between the first gate and the second gate, the third trench having a third depth that is less than the first depth and a third width that is narrower than the first width, and a first device isolating layer and a second device isolating layer in the first trench, the second trench, and the third trench, respectively, the first device isolating layer comprising a first material different from a second material that the second device isolating layer comprises, wherein the first material is located on an upper surface of the second device isolating layer and wherein an upper surface of the first device isolating layer and the upper surface of the second device isolating layer are substantially coplanar.

2. The semiconductor device of claim 1, wherein the first device isolating layer comprises a Tantalum Silicate (TaSi₂) or fluorine chemical vapor deposition (FCVD) oxide, and wherein the second device isolating layer comprises a high density plasma (HDP) oxide or an undoped silicate glass (USG) oxide.

3. The semiconductor device of claim 2, wherein the third device isolating layer comprises nitride, a TaSi₂ or FCVD oxide and has a lower etching resistance than that of the first device isolating layer.

4. The semiconductor device of claim 1, wherein the first device isolating layer has a superior gap fill properties to the second device isolating layer.

5. The semiconductor device of claim 1, wherein the third device isolating layer has a lower etching resistance than that of the first device isolating layer.

6. The semiconductor device of claim 1, wherein an upper portion of a side of the second device isolating layer is in direct contact with the first device isolating layer.

7. The semiconductor device of claim 1, further comprising a fourth device isolating layer and a bottom contact, wherein the second trench comprises a lower portion comprising opposing sides that are laterally bulging.

8. The semiconductor device of claim 1, wherein the first device isolating layer and the second device isolating layer comprise materials different from each other.

9. The semiconductor device of claim 1, further comprising: a first metal gate on the fin and on a side of the first source/drain region, a second metal gate on the fin and on a side of the second source/drain region, the first metal gate and the second gate wherein the fourth device isolating layer comprises a first region and a second region, and a width of the first region is different from a width of the second region.

10. The semiconductor device of claim 1, further comprising: a first metal gate on the fin and on a side of the first source/drain region, a second metal gate on the fin and on a side of the second source/drain region, the first metal gate and the second gate wherein the fourth device isolating layer comprises a first region and a second region, and a width of the first region is different from a width of the second region.

11. The semiconductor device of claim 1, further comprising: a first metal gate on the fin and on a side of the first source/drain region, a second metal gate on the fin and on a side of the second source/drain region, the first metal gate and the second gate wherein the fourth device isolating layer comprises a first region and a second region, and a width of the first region is different from a width of the second region.

12. A semiconductor device comprising: a first trench of a first depth defining a fin, a second trench overlapping with the first trench in plan view and having a second depth that is greater than the first depth, a first gate and a second gate on the fin, the first gate and the second gate traversing the fin and defining a fin, the first trench having a first depth and a first width, a first source/drain region and a second source/drain region on the fin, the first source/drain region and the second source/drain region being adjacent to each other, a third trench in the fin and between the first gate and the second gate, the third trench having a third depth that is less than the first depth and a third width that is narrower than the first width, and a first device isolating layer and a second device isolating layer in the first trench, the second trench, and the third trench, respectively, the first device isolating layer comprising a first material different from a second material that the second device isolating layer comprises, wherein the first material is located on an upper surface of the second device isolating layer and wherein an upper surface of the first device isolating layer and the upper surface of the second device isolating layer are substantially coplanar.

13. The semiconductor device of claim 12, wherein the first device isolating layer comprises a Tantalum Silicate (TaSi₂) or fluorine chemical vapor deposition (FCVD) oxide, and the second device isolating layer comprises a high density plasma (HDP) oxide or an undoped silicate glass (USG) oxide, and wherein an upper portion of a side of the second device isolating layer directly contacts the first device isolating layer.

14. The semiconductor device of claim 12, wherein the third device isolating layer and the third device isolating layer comprise materials different from each other.

15. The semiconductor device of claim 12, further comprising: a first interlayer insulating layer on the first metal gate; and a second interlayer insulating layer on the second device isolating layer, wherein a height of a bottom surface of the first interlayer insulating layer and a height of a bottom surface of the second interlayer insulating layer are the same.

16. The semiconductor device of claim 12, further comprising: a first source/drain region on the fin and on a side of the first metal gate; and a second source/drain region on the fin and on a side of the second metal gate, the first source/drain region and the second source/drain region being adjacent to each other, wherein the second depth is greater than each of a distance between an upper surface of the fin to a lowermost end of the first source/drain region and a distance between the upper surface of the fin to a lowermost end of the second source/drain region.

Take the above image as an example, we can see the changes in protection strategy from one patent family member to another through the words highlighted in red and green. Red meaning text has been altered or removed, and green shows newly added lines or the final changes made to the claims/descriptions.

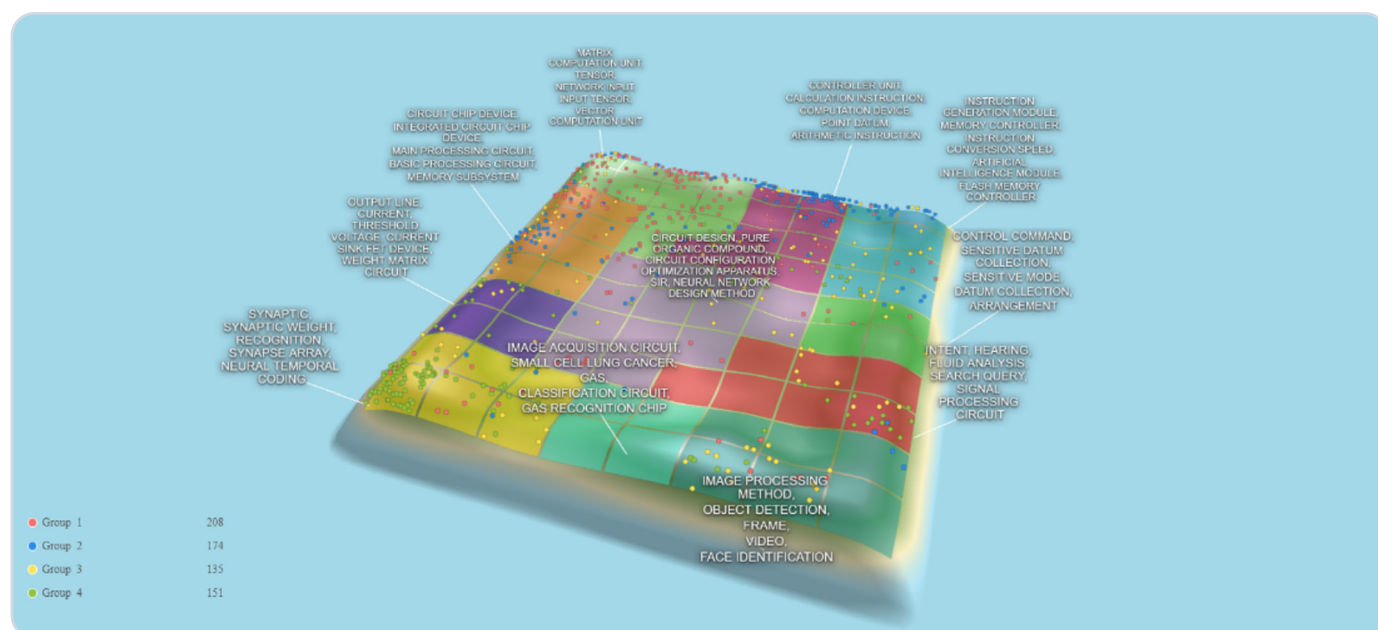
Using CII to Uncover Relevant Analytics:

CII Landscaping Tool:

Landscaping is the most efficient way to assess huge volumes of data related to information contained within patents. Turning this data into a topography that can be visually explored, annotated and interrogated can help you answer questions on whether your proposed inventions or similar inventions have already been patented, what the level of patent activity around specific technologies is and the key actors in those spaces as well as identify white space opportunity for innovation.

In emerging or competitive industries, such as semiconductors, by the time you complete a full research project several weeks may have passed, and by this time new patents may have been filed, changing the landscape and rendering your project outdated. By using an AI-developed 3D landscape, the time to produce or update your reports is dramatically reduced and your resulting map will be dynamically linked to all the patents fitting your search criteria. Your 3D landscape will constantly evolve as more patents are filed, ensuring you always have an accurate depiction of the market you are analyzing.

By visualizing patent density and white spaces, color-coded by variables such as assignee or classification code (IPC, CPC etc.), patterns and trends are more readily pronounced (compared to a narrow research question).



Take the above landscape as an example. Here, the patents for chips optimized for AI with active protection are plotted. The peaks and troughs illustrate areas of high versus low patent density, and the proximity of the dots (patents) indicate document similarity. The red squares represent Google, the blue squares represent Shanghai Cambricon Information Tech Co., the yellow squares represent Intel, and the green squares represent IBM Corp. Based on the grouping of "dots" in the various color-coded sectors, it becomes obvious that IBM currently dominates the region of neural temporal coding, while Google dominates in matrix and vector computation units, and Shanghai Cambricon dominates in Controller units, whereas Intel is evenly spread among the whole landscape.

We can further refine the landscape to see more specific data, understand a company's movement and innovation over time, or see which technology spaces are ripe with opportunities. Plus, grids can be overlaid to define technology areas, as well as assignees, inventors, litigation, valuation or licensing data to help mitigate risk and uncover whitespace.

The complexity of analyzing freedom to operate is multiplied when your innovation falls within a highly specialized domain such as semiconductors, where technical language can make it difficult to understand the key claims and scope of the patent. When all the patents are placed onto a landscape, the most relevant patents (and those which present the greatest risk of infringement to your research) become immediately obvious, as well as your key competitors, meaning you can prioritize your efforts efficiently.



Furthermore, 3D landscape can be used to zero-in on a specific area of interest. By selecting the most relevant areas, it's easy to develop a highly customized landscape. The landscape shown above illustrates the sector related to neural temporal coding and synaptic recognition and highlights additional details and whitespace.

Case Study: Ambature



Liam Kelly,
Strategy & Emerging Technologies Analyst, Ambature

Ambature is an intellectual property licensing company for advanced materials, device architectures, and chip designs within the semiconductor industry. We focus on superconducting materials and quantum devices for sensing, high-performance, and quantum computing applications. PatSnap comprehensively and cost-effectively fulfills several important roles that used to be performed by in-house and external lawyers, enabling us to allocate more resources to research and development.

We primarily use PatSnap to monitor forward citations of our portfolio as well as innovations in relevant markets. Our portfolio is a global one, with hundreds of patent assets issued in ten of the world's major economies. Interacting with individual patent offices or querying public databases is tedious and error-prone. PatSnap provides immediate access to the information we need and organizes our citations in a convenient, consistent, and clear interface. We are automatically notified via email whenever a company cites one of our patents, strengthening or inspiring discussions with potential licensees and prototype partners.

The Advanced Search tool is excellent for finding patents of interest, keeping a pulse on the state of the art, and performing competitive analysis. Nearly half of Ambature's IP portfolio is dedicated to computing and sensing, while the other half is dedicated to clean energy—the generation, transmission, and storage of electricity. We do fundamental research, create IP and chip designs in the area of applied superconductivity, protect our IP via patents and trade secrets, and license that IP directly to end-users or via OEMs. PatSnap helps us see which companies are interested in use cases where we have strong value propositions, and we can directly share interesting publications with members of our science team for review and discussion. In the advanced chip industry, a single product can have many important contributors from wafer material manufacturers, fundamental device designers, memory suppliers, architecture, and interconnect designers to packaging troubleshooters. PatSnap helps us navigate complementary, supplementary, and competitive offerings to strengthen our own technology roadmap and accelerate our go-to-market strategy by identifying high-value partners. We highly recommend PatSnap. – Liam Kelly, Strategy & Emerging Technologies Analyst, Ambature

Charts & Analytics:

CII is more than just search and refinement, it is also exploring industry trends and competitor portfolio shifts through real-time insights on patent activity, new research, and technology areas.

The ability to effectively analyze results is critical for any business. Quality analysis is a key factor when it comes to making the correct decisions for your business, which will not only enable you to survive but also be successful within your technology field. This analysis can also be critical for the results you get when performing a patent search because having knowledge of both your own and your competitors' IP capabilities should be a key consideration when it comes to making many important business decisions.

Using CII and AI graphic analyses on a collection of patents is effortless and can include filing rates, top technology trends, major players in the field, the most competitive jurisdictions, and more.



Continuing with the search above on chips optimized for AI, we see the analytics overview for the active patents. In this example, the number of patent applications is trending upward. Further, the top IPC code in this analysis is G06N3/063 (computer systems based on biological models, using electronic means), the top assignee is IBM, and the most competitive market is the US. You can dive into this data or create different charts based on what you are looking to analyze or compare.

Three points to consider when analyzing results:

1. Be clear about the extraction goal. The more specific you are from the get-go about what information you want to extract, the easier the search is.
2. Locate the charts that enable you to extract the desired data.
3. Collaborate with others to explore the data in more detail and create a 360-degree analysis.

Regardless of industry, these insights can be used to inform key business decisions, including what information to present to potential investors (and when), how to find potential partners or experts in a specific technology space, uncovering emerging trends and competitor activity, and much more.

“

With PatSnap's automatic email notifications, we can easily monitor the IP space, our competitors, customers, and emerging trends. Plus, its Claim Tree, Smart Image, and Workspace tools (to name a few) simplify the patent analysis process saving us ample time. Also, when looking for potential M&A targets, we leverage Insights to understand a company's IP portfolio. Having access to these data points is crucial to our ongoing success, and now we can't imagine not using PatSnap!

”

Claude Carignan,
Senior IP Director & Technical Advisor, Teraxion

Is Connected Innovation Intelligence the right choice for YOU?

By now you're well-versed in how CII is helping semiconductor companies and professionals overcome the hurdles to innovation while protecting IP. Whether your company is a startup looking for licensing opportunities, or a large enterprise organization working to launch the next-generation of chips, CII will help your organization at every stage of the innovation journey. Furthermore, it will enhance your efforts to stay ahead of the competition, increase your ROI, future-proof your operations, and help you bring novel innovation to the market.

If you're looking for an all-in-one solution capable of delivering the innovation insights you need, in a fraction of the time, CII is the right choice for your business.

If you have questions about this guide or CII in general, please get in touch with one of our Innovation experts:

[Connect with an expert.](#)

About PatSnap

Founded in 2007, PatSnap is the company behind the world's leading Connected Innovation Intelligence platform. PatSnap is used by more than 10,000 customers in over 50 countries around the world to access market, technology, and competitive intelligence as well as patent insights needed to take products from ideation to commercialization. Customers are innovators across multiple industry sectors, including Biotechnology, Medical devices, Pharmaceuticals, Chemical, Electronics Manufacturing, Automotive, Consumer Goods, Aviation & Aerospace, Education, Legal Firms.

PatSnap's team of 1000+ employees work from its global headquarters in Singapore, London, and Toronto. To learn more about how PatSnap is improving the way companies innovate, visit www.patsnap.com.

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Additional Resources

Eager to learn more about how CII can aid in semiconductor research and development? Here are several resources you can use on your innovation journey:

The Definitive Guide to Connected Innovation Intelligence: Our #1 Amazon bestselling eBook offers an in-depth overview of CII for innovation across a variety of industries. It offers a walkthrough of the five stages of innovation and explains how CII can help at every stage. [Click here](#) to download your free copy.

Innovation Academy: This free online learning platform features on-demand courses for innovation, R&D, and IP. Innovation Academy is regularly updated and releases new courses every two to four weeks. You can register [here](#).

The Semiconductor Market Report: A detailed 2022 market report featuring insights pulled from PatSnap's CII platform. Includes an IP review, geopolitical supply chain analysis, market context, stakeholder case studies, and much more. Read the full report [here](#).

Connected Innovation Intelligence Success Stories

More than 10,000 companies use CII to innovate successfully. [Click here](#) to learn more and access a wide range of case studies and success stories.



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